

AMENDMENTS TO THE DRAWINGS:

Responsive to the Examiner's requirement that corrected drawings in compliance with 37 CFR 1.121(d) be submitted, Applicants propose adding the legend --Prior Art-- to drawing figures 2A and 2B.

Applicants respectfully request approval.

REMARKS/ARGUMENT

Claims 12-18 are allowed.

Claims 2, 4, 6, 8, 9 and 11 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 2, 4, 6, 8, 9 and 11 have been so amended. Accordingly, Claims 2, 4, 6, 8, 9 and 11 stand allowable.


Rejected Claims 3, 5, 7 and 10 have been amended to depend from allowable claims. Accordingly, Claims 3, 5, 7 and 10 stand allowable.

New Claims 19-23 have been added and depend from allowable claims. Accordingly, Claims 19-23 stand allowable.

Claims 4, 14 and 15 have been amended to overcome the objections.

Claims 12-18 stand allowed. Claims 2-11 and 19-23 stand allowable. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,



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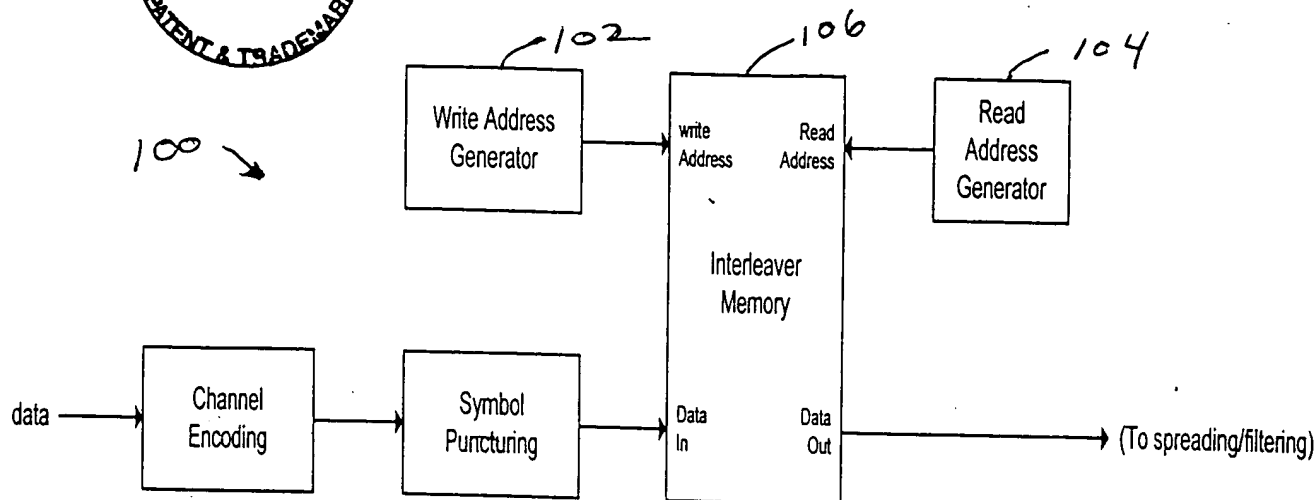
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FIG. 1.



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TI-32201



Prior Art

FIG. 2A

Generic Read Order (A ₀ A ₁ A ₂ A ₃)	Data Input Order (A ₀ A ₁ A ₂ A ₃)	New Write Address - Inverted Generic Read Order (A ₃ A ₂ A ₁ A ₀)
0	0	0
2	1	2
1	2	1
3	3	3
4	4	4
6	5	6
5	6	5
7	7	7
...
31	31	31

4800 or 7200 bps

Generic Read Order (A ₀ A ₁ A ₂ A ₃)	Data Input Order (A ₀ A ₁ A ₂ A ₃)	New Write Address - Inverted Generic Read Order (A ₃ A ₂ A ₁ A ₀)
0	0	0
4	1	2
1	2	4
5	3	6
2	4	1
6	5	3
3	6	5
7	7	7
...
31	31	31

2400 or 3600 bps

Generic Read Order (A ₀ A ₁ A ₂ A ₃)	Data Input Order (A ₀ A ₁ A ₂ A ₃)	New Write Address - Inverted Generic Read Order (A ₃ A ₂ A ₁ A ₀)
0	0	0
8	1	2
1	2	4
9	3	6
2	4	8
10	5	10
3	6	12
11	7	14
...
31	31	31

1800 or 1200 bps

Prior Art

FIG. 2B

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Original row address (A_{or})

32-bit transfer number (TN) 0~17	0	...	5	6	...	11	12	...	17
0	0					1			2
1	3					4			5
2	6					7			8
...									
31	93					94			95

New row address (A_n)

32-bit transfer number (TN) 0~5	0	...	5
0	0		
1	1		
2	2		
...			
95	95		

Prior ART

FIG. 3

